# METHOD AND APPARATUS FOR PROCESSOR CODE OPTIMIZATION USING CODE COMPRESSION


## Abstract of the Disclosure

An improved method of optimizing the instruction set of a digital processor using code compression. In one embodiment, the method comprises obtaining an assembly language program to be used for the optimization process; calculating the static frequency of each instruction type from the base instruction set; sorting the instruction types by frequency; determining the number and type of instructions necessary for correct program execution; creating a compressed instruction set encoding; re-evaluating the compressed instruction according to the foregoing steps; and generating an instruction set encoding for the compressed instruction set. Improved compressed instruction formats and register structures useful in a processor are also disclosed. A computer program and apparatus for synthesizing logic implementing the aforementioned data cache architecture and pipeline performance enhancements are further disclosed.